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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,809	03/18/2004	Hitoshi Saito	042194	5097

38834 7590 02/22/2005

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,809	SAITO, HITOSHI	
	Examiner	Art Unit	
	son t dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 10* is/are rejected.

7)☒ Claim(s) *3,6-9 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

The pre-amendment filed on 3/18/04 has been entered.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirano et al (U.S. Patent No 5,898,608).

For the purpose of this rejection, a dummy cell would be defined as a reference cell because the dummy cell is used as a reference cell in the reading mode of a ferroelectric memory device. See column 1, line 22 of Hirano et al.

With respect to claim 1, figure 8 of Hirano et al disclose a memory device comprising a plurality of ferroelectric capacitors (C0, C254) for memory in which each one end (the left end of capacitor C0) thereof is connected to each of a plurality of first bit lines (every memory cell array must have a plurality of column of bit lines, in this case only BL is shown) via a switching transistor (Qn0), first plate line (the line that

receives signal CP) connected to the other end of the ferroelectric capacitor (C0), first ferroelectric capacitors (each one for each column in a memory cell array, in this case only DC0 is shown) for reference in which one end is thereof is connected to a second bit line (/BL) via a first n-channel MOS transistor (QnD0), a second plate line (the line that receives signal DCP) connected to the other end of the first ferroelectric capacitors (DC0) for reference (see column 7, lines 19-50 for the reading operation of the memory device), and a p-channel MOS transistor (QpC134, figure 13B) connected to the second plate line (DCP). To be more specific, the transistor QpC134 is connected to plate line so as to provide signal DCP to the line, which is connected to the ferroelectric capacitor DC0.

With respect to claim 2, the circuit in figure 13 of Hirano et al is a plate driver circuit (because it generates control signal to the plate line) and transistor QpC134 is clearly formed in a said plate driver circuit and the second plate line are connected.

With respect to claim 4, the switching transistor Qn0 is n-channel MOS transistor.

With respect to claim 5, the sense amplifier SA of Hirano et al clearly amplifies the voltage variation quantity of the first bit line BL and second bit line /BL as disclosed in column 8, lines 1-22 of Hirano et al.

With respect to claim 10, figure 48 of Hirano et al discloses a memory device comprising a memory region of 2T2C type (Qn1, C1, Qn1B, C1B), which stores one bit by first (Qn1) and second (Qn1B) transistors and first (C1) and second (C1B) ferroelectric capacitors, a memory cell region of 1T1C (Qn0 and C0), which stores one bit by a third transistor (Qn0) and a third ferroelectric capacitor (C0) for memory.

Allowable Subject Matter

Claims 3, 6-9 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or suggest a memory device comprising the second ferroelectric capacitors a third plate line and third n-channel MOS transistor with particular connection as claimed in claim 6; a plate driver circuit having a structure that a circuit applies voltage lower than that of the second bit line to a second plate line via a p-channel MOS transistor in an ON state of the p-channel MOS transistor (claim 3); the first ferroelectric capacitors are elements to which data having minus polarization charge is written before heat treatment (claims 8 and 12); the memory cell region of 2T2C is a region corresponding to a range having 1% or less of the number of the bits (claim 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Saigoh et al disclose a 2T2C and 1T1C memory device (figure 1A and 1B).

-Takahashi et al disclose a memory device having a 2T2C cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1969. The fax phone number for the organization where this application or proceeding is assigned is 571-273-1868.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
February 21, 2005

Son T. Dinh
Primary Examiner